Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) An edge node adapted to serve a multiplicity of data streams, said edge node comprising:

a plurality of input ports adapted to receive said data streams, wherein each of said input ports includes an input-port controller and at least one of said input ports includes a bitrate-estimation device adapted to compute a bitrate requirement for each of said data streams;

a plurality of output ports, wherein each of said output ports includes an output-port controller;

a switching fabric adapted to connect any of said input ports to any of said output ports; and

an edge controller including:

an edge control processor adapted to communicate with said plurality of input ports and said plurality of output ports;

a route selection device, in communication with said edge control processor, adapted to select a route for each of said data streams;

a fabric scheduling device, in communication with said edge control processor, adapted to determine a distinct time of transfer for each of a set of data segments, into which each of said data streams are segmented, across said switching fabric; and

a bitrate-allocation device, in communication with said edge control processor, adapted to allocate a bitrate of a data stream based, at least in part, on said

bitrate requirement for said data stream computed by said bitrate-estimation device.

2. (original) The edge node of claim 1 wherein said switching fabric has a greater number of output ports than input ports.

3. (original) The edge node of claim 1 wherein at least one of said output ports includes a time locking device adapted to control a data transmit time from said at least one of said output ports.

4. (original) The edge node of claim 1 wherein said switching fabric is a common-memory fabric.

5. (original) The edge node of claim 1 wherein said switching fabric is a space-switching fabric.

6. (original) The edge node of claim 1 wherein said switching fabric is a rotator-based fabric.

7. (original) The edge node of claim 1 wherein said switching fabric switches entire channels.

8. (original) The edge node of claim 1 wherein said switching fabric switches data segments of time-shared channels.

9. (original) The edge node of claim 1 wherein at least one of said plurality of input ports is a source port adapted to receive data from data sources and at least one of said plurality of input ports is a receiving port adapted to receive data from core nodes and other edge nodes.

10. (original) The edge node of claim 1 wherein at least one of said plurality of output ports is a sink port adapted to transmit data to data sinks and at least one of said plurality of output ports is a departure port adapted to transmit data to core nodes and other edge nodes.

11. (original) The edge node of claim 10 wherein each of said plurality of output ports is adapted to collate said data segments.

12. (original) The edge node of claim 11 wherein said departure port is a time-locking departure port, said time-locking departure port including data buffers and time-locking circuitry.

13. (original) The edge node of claim 1 wherein said bitrate-estimation device is adapted to base said bitrate requirement for each of said data streams on parameters associated with said each of said data streams.

14. (original) The edge node of claim 1 where said bitrate-estimation device further comprises a hysteresis-control device adapted to base said bitrate requirement for each of said data streams on usage measurements associated with said each of said data streams.

15. (original) The edge node of claim 14 wherein said input-port controller further comprises an input buffer and said hysteresis-control device comprises:

an on-off hysteresis-control unit adapted to:

determine an admission state of either accept or reject based on an occupancy of said input buffer; and

reject a request for a new connection for a data stream when said admission state is reject;

an incremental hysteresis-control unit adapted to request bitrate allocation increments.

16-18 (cancelled)

19. (original) An edge node for high-speed traffic processing comprising:

a switching fabric;

a plurality of input ports in communication with said switching fabric, each of said plurality of input ports having an input-port controller;

a plurality of output ports in communication with said switching fabric, each of said plurality of output ports having an output-port controller; and

an edge node controller in communication with said switching fabric, each of said input-port controllers and each of said output-port controllers, said edge node controller including a high-speed scheduling device, said high-speed scheduling device operable to:

receive bitrate allocation information from at least one input-port controller;

maintain a state of a given input port associated with said at least one input-port controller;

maintain a state of each of said plurality of output ports;

assign time slots of a scheduling frame to communicate data segments from said given input port to one or more of said output ports, where the number of said time slots allocated to a given output port is based on said bitrate allocation information; and

transmit said scheduling frame to said corresponding input-port controller.

20. (original) The edge node of claim 19 wherein at least one of said output port controllers further includes a time-locking device for time-locking a corresponding one of said plurality of output ports to a core node.

21. (original) The edge node of claim 19 wherein at least one of said input port controllers comprises a destination identifier adapted to translate an Internet Protocol address.

22. (original) The edge node of claim 19 wherein at least one of said input port controllers includes a data formatter adapted to segment a received data stream into equal sized data segments.

23. (original) The edge node of claim 19 wherein at least one of said input port controllers includes a bitrate allocation requirement estimator adapted to control requests for changes in bitrate allocation.

24. (original) The edge node of claim 19 wherein said input-port controller is adapted to receive a data stream that specifies a destination and an explicit bitrate allocation requirement and wherein said edge node controller is adapted to provide a route to said destination having said explicit bitrate allocation requirement.

25. (original) The edge node of claim 19 wherein said input-port controller is adapted to receive a data stream that specifies a destination and estimate a bitrate allocation requirement

for said data stream and wherein said edge node controller is adapted to provide a route to said destination having said estimated bitrate allocation requirement.

26. (original) The edge node of claim 25 wherein said input-port controller is adapted to

estimate a requirement for bitrate allocation according to a hysteresis-control mechanism; and

transmit a request for a change in said estimated bitrate allocation requirement for said data stream.

27-43 (cancelled)